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built in self test and **re generate** and **compact** and **test result**

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1 [Retargetable self-test program generation using constraint logic programming](#)

Ulrich Bieker, Peter Marwedel

January 1995 **Proceedings of the 32nd ACM/IEEE conference on Design automation**Full text available: [pdf\(60.72 KB\)](#)Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

2 [Novel DFT, BIST and diagnosis techniques: Effective diagnostics through interval unloads in a BIST environment](#)

Peter Wohl, John A. Waicukauski, Sanjay Patel, Greg Maston

June 2002 **Proceedings of the 39th conference on Design automation**Full text available: [pdf\(155.82 KB\)](#)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Logic built-in self test (BIST) is increasingly being adopted to improve test quality and reduce test costs for rapidly growing designs. Compared to deterministic automated test pattern generation (ATPG), BIST presents inherent fault diagnostic challenges. Previous diagnostic techniques have been limited in their diagnosis resolution and/or require significant hardware overhead. This paper proposes an interval-based scan-unload method that ensures diagnosis resolution down to gate-level faults ...

Keywords: built-in self-test (BIST), fault diagnosis

3 [A fast signature simulation tool for built-in self-testing circuits](#)

S. B. Tan, K. Totton, K. Baker, P. Varma, R. Porter

October 1987 **Proceedings of the 24th ACM/IEEE conference on Design automation**Full text available: [pdf\(896.99 KB\)](#)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

This paper describes a Fast Signature Simulator (FSS) tool for Built-In Self-Testing (BIST) circuits. The FSS consists of a simulator generator and a compiled code simulator. The simulator generator comprises a controlling program called the EXECUTIVE and translation software called SIM-GEN. SIM-GEN accepts a Hardware Description Language (HDL) representation of the circuit-under-test as its input and produces C code simulation modules comprising Boolean relations that represent the structure ...